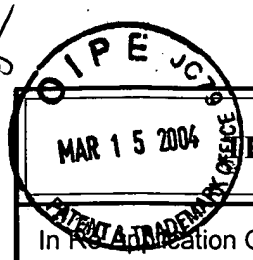
125



AP/2812

TRANSMITTAL OF APPEAL BRIEF (Large Entity)

Docket No. **MCT.0042**

In Re Application Of: **Chandra V. Mouli**

Serial No.	Filing Date	Examiner	Group Art Unit
09/379,092	**August 23, 1999**	**Ron Pompey**	**2812**

Invention: **Forming Sidewall Oxide Layers for Trench Isolation**

TO THE COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on **August 23, 2001**

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Signature

Dated: **March 8, 2004**

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I certify that this document and fee is being deposited on **March 8, 2004** with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Typed or Printed Name of Person Mailing Correspondence

cc:

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Applicant:	Chandra V. Mouli	§	Art Unit:	2812
		§		
Serial No.:	09/379,092	§		
		§	Examiner:	Ron Pompey
Filed:	August 23, 1999	§		
		§		
Title:	Forming Sidewall Oxide Layers For Trench Isolation	§	Docket No.	MCT.0042US
		§		
		§		

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Dear Sir:

Applicant respectfully appeals from the final rejection mailed on June 28, 2001. This brief responds to Paper No. 20040205. That paper indicates claim 33 was rejected under Section 103, but that statement appears to be in error. See *infra.* at VII.

I. REAL PARTY IN INTEREST

The real party in interest is Micron Technology, Inc.

II. RELATED APPEALS AND INTERFERENCES

None.

III. STATUS OF THE CLAIMS

Claims 1-3, 5-7, 33, and 35-39 have been finally rejected and are the subject of this appeal.

IV. STATUS OF AMENDMENTS

No amendments after final have been submitted.

V. SUMMARY OF THE INVENTION

Referring to Fig. 1, a conventional semiconductor layer 10 may be used as the semiconductor structure for forming integrated circuit devices with shallow trench isolation (STI). A dielectric layer 12, commonly called a pad oxide, may be formed over the structure 10. The layer 12 may be formed using any conventional technique including thermal oxidation or deposition. In accordance with conventional silicon trench isolation processes, a nitride layer 14 may be formed over the layer 12. See Specification at page 3, line 22 through page 4, line 11.

An anti-reflective coating 16 may be patterned on top of the nitride layer 14. The anti-reflective coating 16 may be used in advanced lithographic processes to define a pattern for etching through the layers 12 and 14. However, other patterned mask layers may be used, such as those using photoresist.

Referring next to Fig. 2, an anisotropic etching process may be used to form an opening 18 through the nitride layer 14 and the dielectric layer 12 down to the surface of the layer 10.

Next, a solid diffusion source 20 may be deposited into the opening 18. Suitable solid diffusion sources include borophosphosilicate glass (BPSG) materials doped with an oxidation enhancing species such as argon, or other inert species or oxygen. The source 20 allows impurities in the source to diffuse into the layer 10 when exposed to modest temperatures. As a result of the diffusion, the impurities form a diffused region 22 defined by the masking action of the opening 18. See Specification at page 4, line 12 through page 5, line 6.

Through the use of a solid diffusion source, an impurity laden region 22 containing oxidation enhancing impurities may be formed in the layer 10. The region 22 need not

unnecessarily create interface states, generation and recombination centers, or other damage effects which may adversely effect the performance of the resulting STI.

As illustrated in Fig. 4, an anisotropic etch forms a trench 24, which may have substantially vertical sidewalls 25. The anisotrophic etch is masked by the layers 12 and 14, which also act as the mask for the solid source diffusion. Thus, the trench 24 extends through the oxidation enhancing impurity region 22 leaving the portion 22a around the trench 24. The portion 22a corresponds to the underdiffusion which necessarily results in the course of the solid source diffusion process illustrated in Fig. 3.

The amount of underdiffusion and thus the lateral and vertical extent of the region 22a is a function of the concentration of impurities in the source 20 and the time and temperature of the diffusion step. As a result of the fact that the same mask is used for the etch and the diffusion, the region 22a is situated precisely at the corner 23 between the upper surface of the structure 10 and the trench 24. This is precisely the region which may be prone to thin oxide thicknesses, which, in turn, may give rise to leakage currents. See Specification page 5, line 7 through page 6, line 6.

Turning next to Fig. 5, a sidewall oxidation process forms the sidewall oxide 26. Because of the oxidation enhancing affect of the impurities in the region 22a, the thickness of the sidewall oxide 26 at the corner is increased and the corners 23a are substantially rounded as a result of the oxidation process, improving the performance of the sidewall oxide 26. Referring to Fig. 6, a trench filler material 28, such as a deposited oxide, may fill the trench lined by the sidewall oxide 26.

An alternate embodiment of the present invention, shown in Fig. 7, uses ion implantation to form the region 32a which corresponds to the region 22a in the embodiment of Fig. 4. After

the step illustrated in Fig. 2, the resulting structure is exposed to an ion implantation 30. The implant species is preferably a species which enhances oxidation. Suitable species include argon, other inert elements and oxygen. Inert species are desirable because they do not contribute carriers to the semiconductor structure. See Specification page 6, line 7 through page 7, line 5.

The implant acts to enhance oxidation rather than to create crystallographic damage which could cause leakage currents. As a result of lateral straggle, a portion 32a of the implanted region extends under the masking layers 12 and 14. The extent of lateral straggle (species movement transverse to the implant direction) is a function of the dose and implant energy. Generally, about 20 percent of implanted species are subject to lateral straggle.

In some embodiments of the present invention, it may be desirable to use an angled implant to produce the region 32a. By using an angled implant and rotating the layer 10, additional impurities may be caused to enter the region 32a. Of course, it should be understood that the height of the structure produced by the layers 12 and 14 is substantially less than what is depicted in the enlarged drawing of Fig. 7 and therefore the effect of the angled implant may be more substantial than it would appear from Fig. 7. Implant angles as high as 30° may be used in some embodiments. However, even where an angled implant is used, since the regions 32a are shielded below an implant mask they are primarily formed by lateral straggling. See Specification page 7, lines 6-26.

To minimize the amount of crystallographic damage that results from the implant, it is desirable to use a relatively low energy implantation. For example, implantation energies of less than 20 keV are generally desirable and in some embodiments implantation energies of less than 10 keV may be used.

It is known that argon has an effect in enhancing oxidation which is not the result of damage to the silicon substrate. See Semiconductor International, Vol. 22, No. 2, February 1999. It is believed, without limiting the present invention, that the presence of argon makes it easier for oxygen to form oxygen-to-silicon bonds. It is believed that this is due to the fact that the silicon to silicon bond energy is higher than the argon to silicon bond energy so that the argon is more easily replaced if the argon is positioned substitutionally within the lattice. With interstitial argon species, the wave functions of silicon and argon are believed to interact to relax the bond strength.

Again, without limiting the present invention, it is believed that oxygen implants may similarly improve oxidation in a way which is not dependant on crystallographic damage effects. Oxidation is limited by the diffusion of oxygen into silicon and the diffusion of oxygen through any overlying oxidation layers. By implanting the oxygen under the surface of the silicon, it is believed that oxidation may be enhanced by the presence of the oxygen in the silicon structure, separate and apart from any damage created by the implant. See Specification page 8, line 1 through page 9, line 3.

After the implanted region 32 has been formed, the ensuing process steps follow the steps illustrated in Figs. 4-6 and described previously. Namely, a trench 24 is formed through the implanted region 32 leaving the regions 32a, formed at least in part by lateral straggle, to either side of the trench. Thereafter, a sidewall oxide 26 is formed creating the round corners 23a. Finally, as shown in Fig. 6, the trench is filled with the trench filler material 28. See Specification page 9, lines 4-26.

Thus, in accordance with embodiments of the present invention, an oxidation enhancing material may be positioned precisely at the corner where reduced oxidation normally occurs. As

a result, in some embodiments, oxidation may be enhanced without significantly increasing the thermal budget for the process. In some embodiments, oxidation may be enhanced while actually reducing the thermal budget by reducing the temperatures or the times of high temperature steps commonly used in the sidewall oxidation step to overcome the reduced oxidation at the corner. At the same time, it is possible to decrease the disruption of the crystallographic structure at the corner region which would otherwise give rise to the possibility of crystallographic damage, interface states, generation and recombination centers and other defects which may produce leakage currents. See Specification page 10, lines 1-16.

VI. ISSUES

A. Is claim 1 anticipated by Hong?

B. Is claim 33 anticipated by Hong?

VII. GROUPING OF THE CLAIMS

For convenience, claims 2-3 and 5-7 may be grouped with claim 1 and claims 35-39 may be grouped with claim 33. Claim 33 was only rejected under Section 102. See e.g., Examiner's Answer at paragraphs 2 and 4. It appears that the reference to Batra in paragraph 1 of the final rejection was only intended to refer to claims 5-6 and 36-38, as further demonstrated in the Examiner's Answer. Claims 5-6 stand or fall with claim 1 and claims 36-38 stand or fall with claim 33.

VIII. ARGUMENT

A. Is claim 1 anticipated by Hong?

Claim 1 stands rejected under §102 based on the reference to Hong. (The taking of official notice was only with respect to the §103 rejection of the dependent claims.)

Claim 1 calls for implanting impurities that enhance the oxidation of said structure beyond that which would be expected from crystallographic damage effects. The final rejection states that "Hong is silent on what produces the oxidation enhancement by implanting dopant species into the substrate. Therefore, it is not disclosed whether it is crystallographic damage . . ." In view of this statement, it is clear that the §102 rejection of claim 1 is not appropriate.

In the Advisory Action, it is stated that Hong discloses that "since the regions at the upper corners of the trench are doped, the degree of oxidation there is enhanced." But again, Hong is silent (as the Examiner has already admitted) on what produces the enhancement. It is clear that in the summary cited by the Examiner, all the reference means by doped is that the ions are implanted. See column 2, lines 53-55. ("Then, ions are implanted at an tilt-angle into the non-active region of the substrate to form a doped region using the mask layer as a hard mask.") What is unstated is whether the enhancement is due to crystallographic damage effects or some other effect. Thus, as the Examiner has already stated, Hong is silent on what produces the oxidation enhancement and the claims specifically require a specific type of oxidation enhancement.

As already admitted (correctly) by the Examiner, Hong is silent on the critical point set forth in the claims.

Therefore, the §102 rejection of claim 1 should be reversed.

B. Is claim 33 anticipated by Hong?

Claim 33 stands rejected under §102 based on the reference to Hong. (The taking of official notice was only with respect to the §103 rejection of the dependent claims.)

Claim 33 calls for defining an opening in a masking layer over semiconductor structure and causing impurities to enter a portion of said structure through the opening to enhance the oxidation of said structure beyond that which would be expected from the crystallographic

damage effects. Therefore, for the reasons described above, the §102 rejection of claim 33 is also inappropriate and should be reversed.

VIV. CONCLUSION

Applicant respectfully requests that each of the final rejections be reversed and that the claims subject to this Appeal be allowed to issue.

Respectfully submitted,

Date: March 8, 2004

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APPENDIX OF CLAIMS

The claims on appeal are:

1. A method of forming a trench isolation comprising:

forming a region containing oxidation enhancing impurities in a semiconductor structure by implanting impurities which enhance the oxidation of said structure beyond that which would be expected from crystallographic damage effects; and

making a trench through said region, leaving a portion of said region around said trench.

2. The method of claim 1 wherein forming said region includes forming said region using ion implantation.

3. The method of claim 2 wherein using ion implantation includes using implantation at energies below 20 keV.

5. The method of claim 1 further including implanting argon.

6. The method of claim 1 further including implanting oxygen.

7. The method of claim 3 wherein using implantation further includes using an angled ion implant.

33. A method of forming a trench isolation comprising:

defining an opening in a masking layer over a semiconductor structure;

causing impurities to enter a portion of said structure through said opening to enhance the oxidation of said structure beyond that which would be expected from crystallographic damage effects; and

using said mask to form a trench through the portion of said structure containing said impurities.

35. The method of claim 33 wherein causing impurities to enter said semiconductor structure includes ion implanting said impurities.

36. The method of claim 35 including implanting inert impurities.

37. The method of claim 36 including implanting argon.

38. The method of claim 35 including implanting oxygen.

39. The method of claim 35 including ion implanting at energies of less than 20 keV.